B. P. Poddar Institute of Management & Technology

Department of Electronics & Communication Engineering

Academic Year: 2018-19, Semester: Odd

4 ECE 7th semester

Laboratory Name: Hamming Laboratory Room No.: B 603

Course Name: VLSI Design Laboratory (EC792)

List of Experiments to be conducted

Sl. No.	Name of Experiment	CO	PO	PSO
1.	Familiarity with Spice simulation tool, Layouts, Transistors and tools. Familiarity with EDA tools for VLSI design/ FPGA based system design.	1,2,3	1	1,2
2.	Spice Simulation of Inverter, Nand, Nor Gates.	2	1,2,5	1,2
3.	Design of CMOS X-OR/X-NOR Gates.	2	1,2,5	1,2
4.	Design of CMOS Full adder.	2	1,2,3,5	1,2
5.	Design of CMOS Flip flops (R-S, D, and J-k).	2	1,2,3,5	1,2
6.	Standards Cell design.(inverter fabrication)	3	1,5	1,2
7.	Design of 8 bit Synchronous Counter.(VHDL programming)	1,4	1,2,3,5,6	1,2
8.	Design of an 8 bit bi-direction register with tri-stated output bus.	1,4,5	1,2,3,5,6,7	1,2
9.	Design of a 8 bit ALU with few instructions and implementation and validation on FPGA.	4,5	1,2,3,4,5,6,7	1,2
10.	One Beyond syllabus experiment: a. Design a 4 bit data in/out RAM for CPU using VHDL and validation on FPGA.	1,4	1,2,3,4,5,6,7	1,2
	b. Transfer Characteristic of CMOS inverter for different values of β (β < 1, β = 1, β > 1).	2,5	1,2,3,4,5,6,7	