B. P. PODDAR INSTITUTE OF MANAGEMENT & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
LABORATORY NAME: VON NEUMANN LAB(C409)
ACADEMIC YEAR: 2018-2019 ODD SEMESTER
LIST OF EXPERIMENTS

COMPUTER ORGANIZATION(CS393)

TOPIC	LIST OF EXPERIMENTS	CO	PO/ PSO
1.Introduction Lab	1. Introduction to Computer Organization Lab and Digital Trainer Kit. 2. Truth Table verification of all basic logic gates. 3. Implement Basic gate using Universal Gates.	CO1	PO1, PO8, PO10, PO12,PSO1
2. Familiarity with IC-chips, e.g. a) Multiplexer , b) Decoder, c) Encoder b) Comparator Truth Table verification and clarification from Data-book.	1. Truth Table Verification and Application of Multiplexer. 2. Truth Table Verification and Application of Decoder. 3. Truth Table Verification of Encoder and Comparator.	CO2	PO1, PO2, PO8, PO10, PO12,PSO1,PSO2
3. Adder/Subtractor	Design of an Adder/Subtractor Composite Unit (Ripple Carry Adder).	CO3	PO1, PO2, PO3, PO4, PO8,PO9,PO10,PO12, PSO2
4.BCD Adder	Design a BCD Adder.	CO3	PO1, PO2, PO3, PO4, PO8,PO9, PO10,PO12, PSO2

5.Carry Look Ahead Adder	Design of a 'Carry-Look-Ahead' Adder circuit.	CO3	PO1, PO2, PO3, PO4, PO8,PO9,PO 10,PO12, PSO2
6.ALU	Use a multiplexer unit to design a composite ALU.	CO4	PO1, PO2, PO3, PO8,PO9, PO10,PO12, PSO2
7.ALU	Implement multibit arithmetic operation using ALU chip.	CO4	PO1, PO2, PO3, PO8,PO9, PO10,PO12, PSO2
8.RAM	Verification of RAM chip using IC 7489.	CO5	PO1, PO2, PO3, PO4, PO8,PO9,PO 10,PO12, PSO2
9.Beyond Syllabus	1.Implement Half Adder, Full Adder using Basic Gates. 2.Implemen Half Subtractor, Full Subtractor using Basic Gate.	CO3	PO1, PO2, PO3, PO4, PO8,PO9,PO 10,PO12, PSO2