Model Question Paper

Microelectronics &VLSI Design

Time Allotted: 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for *any ten* of the following : 10×1=10

i. Pseudo NMOS logic provides which of the following advantages?

a) Static power dissipation is less compared to CMOS logic

b) It is much faster compared to other logics

c) It requires less no. of transistors compared to CMOS logic

d) It is more noise immune.

ii. Which type of MOSFET exhibits no current at zero gate voltage?
a. Depletion MOSFET b. Enhancement MOSFET c. Both a and bd. None of the above

iii. For a symmetrical CMOS inverter the relation between aspect ratio of NMOS and PMOS is

a) $(W/L)_P = (W/L)n$ b) $(W/L)_P = 2.5(W/L)n$ c) $2.5(W/L)_P = (W/L)n$ d) $(W/L)_P = 1/2.5(W/L)n$

iv. Advantage of SRAM over DRAM is:

a) Very high speed. b) Low cost per bit

c) Higher density d) Less space required

v. Hierarchical decomposition of a large system in VLSI design is called

a) Modularity b) Regularity c) Locality d) Decomposability

vi. What is the full form of FPGA ?
a) Field programmable gate array..
b) Full programmable gate array.
c) Fast programmable gate array .

vii. For a 2 inputs XOR gate what is the maximum nos. of MOS transistor.
a) 16 b)8 c)6 d)10

vii. Which is not a part of FPGA?
a) Configurable logic block.

b) IOB.
c) Microprocessor.
d) Routing Channels.

viii. Which are the simple PLDS?
a) CPLD. b)FPGA. c)CBIC. d)PLA.

ix. How many CMOS Transistors are needed to implement XOR gates?
a) 7 b)10 c)8 d)9

x. What is ASIC?

a) Application simplified IC. b) Applied IC. c) Application specific IC.

d) Authentic IC.

xi. VLSI design flow is a

a) cyclic process only b)parallel process c) sequential & cyclic process

d) none of these

xii. VHDL is a

a) Multi threaded program b) language like C c) single user program

GROUP – B
(Short Answer Type Questions)

Answer *any three* of the following. 3×5=15

2. Explain the operation of CMOS inverter with proper voltage transfer characteristic.

3. Explain how ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.

4. Produce the XOR gate with 6 transistors CMOS TG.

5. Calculate the threshold voltage of a CMOS inverter.

6. Implement the following Boolean function with PLA

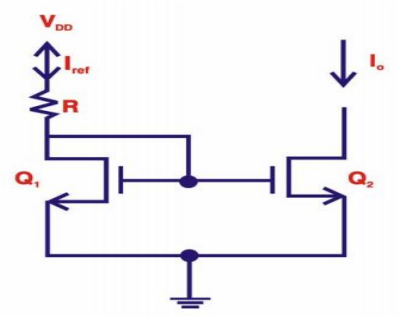
a) Y=ab + bc +ca
b) F= ab’ + abc’

GROUP – C
(Long Answer Type Questions)

Answer *any three* of the following. 3×15=45

7. a. Explain the n- well CMOS fabrication process with necessary diagram. 5

b.



Let V_{DD} = 5V, $V_{TH,1}$ = 1V, $k_{n,1}'$ = 20 μ A/V² and R = 1K Ω .
What should be $(W/L)_1$ needed for creating I_{ref} = 1mA? 5

c. Classify ASIC. Explain briefly the different ASIC. 5

8. a. Design AND , XOR gates using pass transistor logic. 5

b. design CMOS master slave D FF and describe its operation. 5

c. what do you mean by DCVSL design explain briefly with example. 5

9. a. Draw the VTC and explain different regions of CMOS inverter. Deduce the threshold voltage of CMOS inverter . 7+8

10. a. explain the pre-charge and evaluation for dynamic CMOS. 5

b. deduce the CMRR of CMOS differential amplifier. 10

11. a. explain the terms entity and architecture of VHDL program. 3

b. write a program to develop up counter using JK Flip flop using VHDL. 7

c. Explain the procedure of writing operation using SRAM.

12. Write short notes on the following:

a) Explain is Channel-length modulation.
b) VHDL modeling of D-flip/flop.
c) Channel routing.
d) Layout of CMOS inverter.
e) Explain the FPGA architecture